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1. An electrostatic discharge circuit connected between a first power supply voltage source and a second power supply voltage source to protect internal integrated circuits from damage due to an electrostatic discharge, said electrostatic discharge circuit comprising:

a plurality of serially connected polycrystalline silicon diodes formed on a surface of a substrate, each diode having a first electrode and second electrode, said plurality of serially connected polycrystalline diodes including a first diode of the plurality of diodes has its first electrode connected to the first power supply voltage source, and a last diode having its second electrode connected to the second power supply voltage source,

wherein the first electrode is a first region of a polycrystalline silicon being heavily doped with an impurity of a first type and the second electrode is a second region of a polycrystalline silicon being heavily doped with an impurity of a second type, said second region being adjoined to the first region to form an electrical junction.

2. The electrostatic discharge circuit of claim 1 wherein the adjoined first and second regions of each diode are formed on shallow trench isolation formed within the substrate.

3. The electrostatic discharge circuit of claim 1 wherein each diode further comprises a resistor protection oxide formed to overlay a portion of the first and second regions at the junction.

4. The electrostatic discharge circuit of claim 1 wherein the first electrode of each polycrystalline silicon diode is a cathode and the second electrode of each polycrystalline silicon diode is an anode.

5. The electrostatic discharge circuit of claim 4 wherein the impurity of the first type is an N-type impurity having a density of from approximately 10^{15} atoms/cm^{-3} to approximately 10^{21} atoms/cm^{-3}.

6. The electrostatic discharge circuit of claim 4 wherein the impurity of the second type is a P-type impurity having a density of from approximately 10^{15} atoms/cm^{-3} to approximately 10^{21} atoms/cm^{-3}.

7. The electrostatic discharge circuit of claim 4 wherein each of the polycrystalline diodes has a thickness of from approximately 1000Å to approximately 3000 Å.

8. The electrostatic discharge circuit of claim 4 wherein each of the polycrystalline diodes has a thickness of from approximately 0.5μm to approximately 100μm.

9. The electrostatic discharge circuit of claim 1 wherein a number of the plurality of serially connected polycrystalline silicon diodes is determined by the formula:

$$n \geq \frac{V_{noise} + |Vx1 - Vx2|}{V_T}$$

where:

n is the number serially connected of polycrystalline silicon diodes,

V_{noise} is the maximum voltage level difference allowed to be present on the internal integrated circuits between the first power supply voltage source and the second power supply voltage source,

Vx1 is the magnitude of the first power supply voltage source,

Vx2 is the magnitude of the second power supply voltage source, and

V_T is the threshold voltage of each polycrystalline silicon diodes.

10. An integrated circuit formed on a substrate comprising:

a first power distribution network connected to a first power supply voltage source;

a second power distribution network connected to a second power supply voltage source;

a plurality of internal circuits connected between the first and second power distribution networks; and

an electrostatic discharge circuit connected between a first power supply voltage source and a second power supply voltage source to protect said internal circuits from an ESD event, said electrostatic discharge circuit comprising:

a plurality of serially connected polycrystalline silicon diodes formed on a surface of a substrate, each diode having a first electrode and second electrode, said plurality of serially connected polycrystalline diodes including a first diode of the plurality of diodes has its first electrode connected to the first power supply voltage source, and a last diode having its second electrode connected to the second power supply voltage source,

wherein the first electrode is a first region of a polycrystalline silicon being heavily doped with an impurity of a first type and the second electrode is a second region of a polycrystalline silicon being heavily doped with an impurity of a second type, said second region being adjoined to the first region to form an electrical junction.

11. The integrated circuit of claim 10 wherein the adjoined first and second regions of each diode are formed on shallow trench isolation formed within the substrate.

12. The integrated circuit of claim 10 wherein each diode further comprises a resistor protection oxide formed to overlay a portion of the first and second regions at the junction.

13. The integrated circuit of claim 10 wherein the first electrode of each polycrystalline silicon diode is a cathode and the second electrode of each polycrystalline silicon diode is an anode.

14. The integrated circuit of claim 13 wherein the impurity of the first type is an N-type impurity having a density of from approximately 10^{15} atoms/cm^{-3} to approximately 10^{21} atoms/cm^{-3}.

15. The integrated circuit of claim 13 wherein the impurity of the second type is a P-type impurity having a density of from approximately 10^{15} atoms/cm^{-3} to approximately 10^{21} atoms/cm^{-3}.

16. The integrated circuit of claim 13 wherein each of the polycrystalline diodes has a thickness of from approximately 1000Å to approximately 3000 Å.

17. The integrated circuit of claim 13 wherein each of the polycrystalline diodes has a thickness of from approximately 0.5μm to approximately 100μm.

18. The integrated circuit of claim 10 wherein a number of the plurality of serially connected polycrystalline silicon diodes is determined by the formula:

$$n \geq \frac{V_{noise} + |Vx1 - Vx2|}{V_T}$$

where:

n is the number of serially connected polycrystalline silicon diodes,

V_{noise} is the maximum voltage level difference allowed to be present on the internal integrated circuits between the first power supply voltage source and the second power supply voltage source,

Vx1 is the magnitude of the first power supply voltage source,

V_{x2} is the magnitude of the second power supply voltage source, and

V_T is the threshold voltage of each polycrystalline silicon diodes.

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